ABSTRACT

A voltage regulator having an input terminal and an output terminal. A PMOS transistor connects the input terminal to an intermediate terminal. The PMOS transistor includes a first gate oxide layer. An LDMOS transistor connects the intermediate terminal to ground. The LDMOS transistor includes a second gate oxide layer. A controller drives the PMOS transistor and the LDMOS transistor to alternately couple the intermediate terminal between the input terminal and ground, to generate an intermediate voltage at the intermediate terminal having a rectangular waveform. A filter is disposed between the intermediate terminal and the output terminal to convert the rectangular waveform into a substantially DC voltage at the output terminal.